REMARKS

1
2

3   The Applicants respectfully request reconsideration and allowance of claims 1-18 in view

4   of the following arguments.

5

6   INTERVIEW SUMMARY

7   The Applicants appreciate the telephone interview conducted January 11, 2005, between

8   Examiner Sharon, his supervisor, and the undersigned attorney. In the interview, the undersigned

9   attorney summarized the arguments presented below and emphasized the fundamental

10   distinctions between the Teene patent (U.S. Patent No. 6,272,668, hereinafter referred to as

11   "Teene") and Applicants' claims. The general difference between Teene and Applicants' claims

12   were discussed as well as some of the particular differences between the static timing analysis of

13   Applicants' claims and the analysis conducted in Teene. Specifically, Teene's use of automatic

14   analysis in post-layout circuit design was discussed in relation to Applicants' static timing

15   analysis techniques. No agreement was reached as to the allowability of the claims.

16

17   CLAIMS 1-18 ARE NOT ANTICIPATED BY THE CITED PRIOR ART

18   The Examiner rejected claims 1-18 under 35 U.S.C. § 102(e) as being anticipated by

19   Teene. The Applicants respectfully submit that the claims are not anticipated by this reference.

20

21   The Teene Patent

22   Teene discloses a system that relies on "statistical, historical information" to determine

23   the timing of an application specific integrated circuit (ASIC) rather than relying on static timing

24   analysis tools for the ASIC design (col. 6, lines 18-24). In other words, although the Teene

1   patent is directed to a system for improving timing performance of a standard cell ASIC layout,

2   Teene improves the timing performance by testing post-layout timing performance to determine

3   whether to swap circuit cells of an ASIC layout (col. 5, lines 17-21).

4

5   <u>The Teene Patent Fails to Teach Each Element Required in the Respective Claims</u>

6   Applicants' independent claim 1 is directed to a method for analyzing an electronic

7   circuit and requiring the following events:

8   (a)   replacing at least one timing determinant block in a first functional component of
9   the circuit with a timing element set;
10   (b)   performing a circuit simulation for a cross-section of the first functional
11   component to determine timing characteristics associated with each replaced
12   timing determinant block of the first functional component;
13   (c)   attaching the timing characteristics associated with each replaced timing
14   determinant block to the respective timing element set which replaced the
15   respective timing determinant block, thereby creating a timing model for the first
16   functional component; and
17   (d)   performing a static timing analysis for the circuit utilizing the timing model for
18   the first functional component.
19

20   The Examiner appears to liken Teene's swapping of standard cell components with other

21   functionally equivalent standard cell circuit components at col. 11, lines 63-67 to "replacing at

22   least one timing determinant block in a first functional component of the circuit with a timing

23   element set" as required in Applicants' claim 1 at element (a). However, Teene's swapping of

24   standard cell components for functionally equivalent standard cell circuit components is different

25   than replacing a timing determinant block with a timing element set because the timing

26   determinant block is completely removed from the timing model that is eventually created

27   according to the present invention, and not swapped for another timing determinant block.

28   Teene's cell swapping is merely to improve the timing slack value on each timing arc in a sorted

29   list of timing arcs (col. 11, lines 66-67). On the other hand, Applicants claim replacing a timing

1   determinant block with a timing element set. The timing element set of Applicants' claims

2   reduces the processing that would otherwise be required to perform a static timing analysis of an

3   electronic circuit when compared to using a new or swapped cell circuit component as per Teene.

4   In other words, Teene swaps cells to find the "optimum timing slack value" (col. 12, line 3)

5   rather than replace a cell with a timing element set to create a timing model for a static timing

6   analysis.

7   The Examiner also appears to liken Teene's computing of "temporary variables" for use

8   in the analysis of standard cell circuit components at col. 15, lines 37-43 to "performing a circuit

9   simulation for a cross-section of the first functional component" as required in Applicants' claim

10   1, element (b). Applicants' note that the circuit simulation of element (b) is "to determine timing

11   characteristics associated with each replaced timing determinant block." However, as discussed

12   above, Teene swaps cells to find the optimum timing slack value. This computing of temporary

13   slack values cannot be considered to be performing a circuit simulation for a cross-section of the

14   first functional component because Teene's computing of the temporary variables is not

15   simulation of a cross section at all.

16   Also in the Office Action, the Examiner refers to the "two temporary values used to

17   evaluate the possible improvement in timing slack caused by swapping the equivalent cell for the

18   current cell" at col. 16, lines 5-7 in Teene as disclosing element (c) of Applicants' claim 1. This

19   disclosure cannot teach "attaching the timing characteristics associated with each replaced timing

20   determinant block to the respective timing element set which replaced the respective timing

21   determinant block" as required in Applicants' claim 1 at element (c) because in Teene, no timing

1   determinant block is replaced by a timing element set and thus, no timing characteristic in Teene

2   can be attached to any timing element set.

3   Regarding element (d) of Applicants' claim 1, the Examiner points to col. 16, lines 7-15

4   in Teene in an attempt to show performing a static timing analysis for the circuit. However,

5   nothing in Teene discloses performing a static timing analysis utilizing a timing model that

6   includes a timing element set that replaced a timing determinant block as required by element (d)

7   of Applicants' claim 1. In addition, Teene discourages the use of static timing analysis tools

8   when, for example, Teene states that prior art "reliance on static timing analysis renders the

9   method [of automating ASIC layouts] less useful to ASIC designs" (Teene, col. 3, lines 18-65

10   with specific attention to lines 57-59).

11   For the above reasons the Teene reference fails to teach or suggest any of the four

12   elements required in claim 1. Thus, Applicants urge the Examiner to withdraw the § 102

13   rejection of independent claim 1 as being anticipated by Teene. Likewise, claims 2-7 depend

14   from claim 1 and the limitations of claim 1 apply to claims 2-7. Thus, the Examiner is urged to

15   withdraw the § 102 rejection of claims 2-7.

16   Regarding, Applicants' independent claims 8 and 14 with their respective dependent

17   claims, Applicants respectfully submit that these claims require similar limitations as found in

18   claims 1 through 7. Thus, the arguments presented above with respect to claim 1 apply with

19   equal force to independent claims 8 and 14 and their respective dependent claims.

20

Page 5 of 6

1   CONCLUSION

2   For all of the above reasons, the Applicants respectfully request reconsideration and

3   allowance of claims 1-18.

4   If any issue remains as to the allowability of these claims, or if a conference might

5   expedite allowance of the claims, the Examiner is asked to telephone the undersigned attorney

6   prior to issuing a further action in this case.

7

8   Respectfully submitted,

9   THE CULBERTSON GROUP, P.C.

10

11   Dated: ___15 Feb 2005___   By:_____

12   Russell D. Culbertson, Reg. No. 32,124
13   Russell C. Scott, Reg. No. 43,103
14   Trevor Lind, Reg. No. 54,785
15   1114 Lost Creek Boulevard, Suite 420
16   Austin, Texas 78746
17   512-327-8932
18   ATTORNEYS FOR APPLICANTS
19
20   CERTIFICATE OF FACSIMILE
21
22   I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office, (Fax
23   No. 703-872-9306) on February 15, 2005.
24
25   Russell C. Scott, Reg. No. 43,103 _____
26
27

1058_Resp to OA_2004_11_18_filed.wpd

Page 6 of 6